Short Papers

Analytical Nonlinear HEMT Model for Large Signal Circuit Simulation

Takuma Tanimoto

Abstract—**A new nonlinear high electron mobility transistor (HEMT) model based on Curtice model is described. This model introduces term for leakage current for subthreshold bias, drain voltage dependencies of knee voltage, drain conductance and threshold voltage, transconductance enhancement at high frequencies caused by DX centers, and the bias dependence of capacitance. Applying this model to pseudomorphic double-recessed gate HEMT's, average error of 2.6% for dc current and 10% for S-parameters yields.**

I. Introduction

The high electron mobility transistor (HEMT [1]) has been shown to be suitable for low noise circuits at high frequencies and for very high speed circuits. However, their applications is limited for small signal circuits, and there are still few reports concerning large signal circuits, such as mixers and power amplifiers [2].

For the design of large signal circuits, SPICE and nonlinear harmonic balance (HB) simulators are usually adopted. SPICE is a useful simulator because if requires only a few model parameters. However, nonlinear circuit characteristics are not easily calculated, because SPICE works in the time-domain only. HB simulators, on the other hand, are widely used for nonlinear circuit simulation because they work in the frequency domain for nonlinear circuit elements. Nevertheless, the accuracy of HB simulation of nonlinear circuits is still low, because it is limited by active device models.

There are two types of FET device models. One type is the physics-based model, such as classical transport model [3], and so on. These models can deal with limited device characteristics such as transconductance and capacitance. However, they are too complicated to adopt HB simulation. The other type of models is the numerical equation based model, which includes the Curtice model [4] and the Statz model. These models are easily adopted to HB simulation which makes it possible to simulate nonlinear circuit characteristics. These models, however, result in low accuracy for nonlinear simulations because of the formulation used in the model. Some improved nonlinear models have been demonstrated [5], the accuracy of these models are improved for limited region, i.e., satulated region, but accuracy problem remains.

This paper describes a new nonlinear HEMT model based on the Curtice cubic model to obtain highly accurate nonlinear simulation.

II. DC Model

The new model is based on the Curtice model. This model consists of simple functions which are continuous for any order of differentials and which do not diverge for large value of variables. Former property is important for reducing simulation time and improving accuracy of simulation such as harmonic distortion characteristics, while latter is necessary for simulation convergence.

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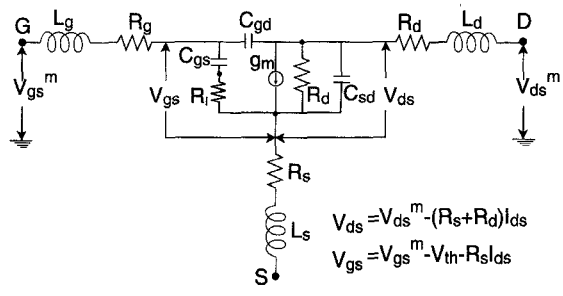

Fig. 1. Equivalent circuit of HEMT adopted in this model.

First, the subthreshold current due to substrate leakage current and short channel effect, which has been neglected in a previous HB models, have been take into account.

To represent dc characteristics below the threshold voltage, a new current term, $I_{\rm ds}^{\rm poly}$, is introduced in the drain current equation

$$I_{\rm ds} = I_{\rm ds}^{\rm poly} + I_{\rm ds}^{\rm leak} \tag{1}$$

$$I_{\rm ds}^{\rm leak} = \frac{a_0 \exp(a_1 V_{\rm gs})}{1 + a_2 a_0 \exp(a_1 V_{\rm gs})} \tag{2}$$

$$I_{\rm ds}^{\rm poly} = \beta(1 + \gamma V_{\rm ds}) \tanh(\alpha V_{\rm ds}) \qquad (V_{\rm gs} > 0) \tag{3}$$

where

$$V_{\rm ds} = V_{\rm ds}^m - (R_s + R_d) \tag{4}$$

$$V_{\rm gs} = V_{\rm gs}^m - V_{\rm th} - R_s I_{\rm ds}. \tag{5}$$

The biases and equivalent circuits adopted for this model are shown in Fig. 1. The $V_{\rm ds}^m$ and $V_{\rm gs}^m$ are the measured (extrinsic) drain bias and gate bias; $V_{\rm ds}$ and $V_{\rm gs}$ are intrinsic drain bias and gate bias; $V_{\rm th}$ is the drain bias dependent threshold voltage. The other symbols are adjustable parameters. Subthreshold drain current is introduced as (2), which is identical to Shottky forward current. According to this equation, in the subthreshold region, drain current is assumed to decay exponentially with $V_{\rm gs}$ from the value $a_0/(1 + a_2 a_0)$ at the threshold voltage, and suppressed for larger gate voltages allow so that convergence of simulation.

Equation (3) is identical to those of Curtice's. However, drain current dependence of threshold voltage $V_{\rm th}$, drain conductance factor γ and knee voltage factor α are introduced in this model as follows:

$$V_{\rm th} = V_{\rm th0} - \delta V_{\rm ds} \tag{6}$$

$$\gamma = \gamma_3 - \gamma_0(1 + \gamma_1 V_{\rm gs}) \tanh\{\gamma_2 V_{\rm gs}\} \tag{7}$$

$$\alpha = \alpha_0 + \alpha_1 \exp\left\{-\left(\frac{V_{\rm gs} - \alpha_2}{\alpha_3}\right)^2\right\}. \tag{8}$$

The drain bias dependence of threshold voltage as expressed in (6) is dominant mainly in the low current regions of the *I-V* characteristics. This factor strongly affects the design of low current operation amplifiers. Next, the gate bias dependence of γ has also been taken into account, as in (7). In previous models, drain conductance has a large gate bias dependence through factor β, as shown in (2). This dependence causes serious errors for the simulated result in the

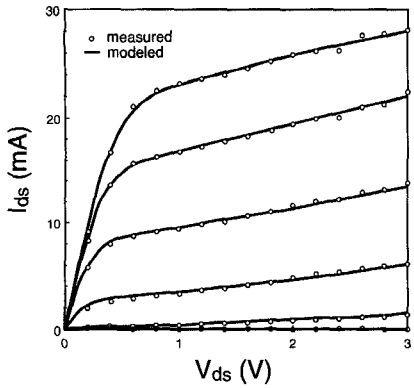

Fig. 2. DC characteristics of measured and modeled results. The open circle indicates the results from measurement, the solid line indicates the results from our model.

gain characteristics of the amplifier. This function is made to decay for larger gate voltages, which counteracts the drain conductance enhancement through the gate bias dependence of β. The drain bias dependence in a is also serious problem for device characteristics, mainly for efficiency. In many devices, knee voltage increases monotonically with gate voltage, but some devices have the inverse dependence. To describe this relationship, a Gaussian distribution was found as a suitable function.

Next, fourth-order polynomials are adopted for the denominator in β

$$\beta = \frac{\beta_1 V_{\rm gs}^2}{1 + \beta_2 V_{\rm gs} + \beta_3 V_{\rm gs}^2 + \beta_4 V_{\rm gs}^3 + \beta_5 V_{\rm gs}^4}. \tag{9}$$

In the *I-V* characteristics of HEMT's, transconductance drop has been observed at high gate voltages. It was found by varying the order of the polynomials that a fourth-order is sufficient to obtain good agreement between modeled and measured characteristics.

Double-recessed 0.15 μm T-shaped gate HEMT's [6] were considerd in this paper. A typical drain current to drain voltage relationship is shown in Fig. 2. Excellent agreement is obtained for wide range of biases. Even in the subthreshold region, the $I_{\rm ds}$ error does not exceed 50%; in a wide area for gate voltages larger than $V_{\rm th}$, the average error is as small as 2.6%.

III. RF Model

Transconductance is usually defined by the $V_{\rm gs}$ differential of drain current defined by (1). The transconductance has dispersion in ordinary FET's. This dispersion decreases as frequency increases. HEMT's have the opposite type of dispersion because of the existence of deep trap levels in the AlGaAs layer (DX centers) [7]. To model this increase due to DX centers, we introduced a new current source $I_{\rm ds}^{\rm rf}$ in the following way:

$$I_{\rm ds}^{\rm rf} = \beta_{\rm rf} \tanh(\alpha V_{\rm ds}) \tag{10}$$

$$\beta^{\rm rf} = \frac{\beta_1^{\rm rf} V_{\rm gs}^2}{1 + \beta_2^{\rm rf} V_{\rm gs} + \beta_3^{\rm rf} V_{\rm gs}^2 + \beta_4^{\rm rf} V_{\rm gs}^3 + \beta_5^{\rm rf} V_{\rm gs}^4} \qquad (V_{\rm gs} > 0). \tag{11}$$

Equations adopted to this RF current source are identical that of dc current as shown in (3) and (9) except drain conductance term γ is neglected. The equivalent circuit with the RF current source is shown in Fig. 3.

The bias dependence of intrinsic capacitances are separated into a drain bias dependent part and a gate bias dependent part as

$$C_{\rm gs} = (1 - \delta) C_{\rm gs0} + \delta C_{\rm gs1} \tag{12}$$

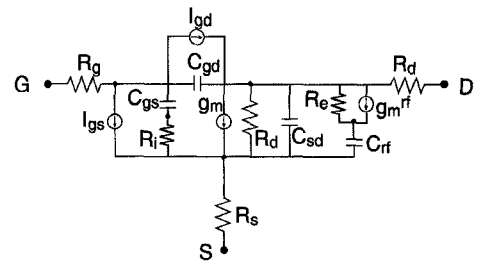

Fig. 3. A new equivalent circuit with DX center induced current source.

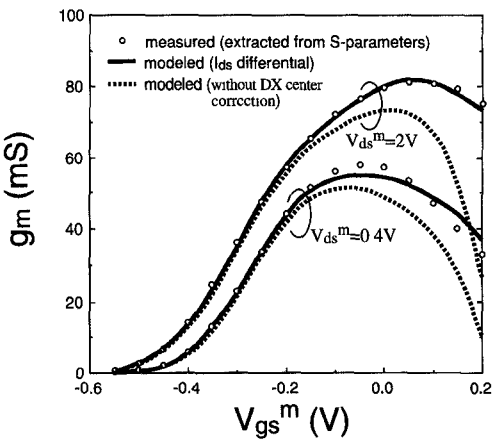

Fig. 4. Comparison of measured and RF modeled (with [solid] and without [dotted] DX center correction) transconductances.

where

$$\delta = \tanh(\alpha V_{\rm ds}) \tag{13}$$

$$C_{g0} = C_{g04} + C_{g03} V_{\rm gs} + C_{g02} \tanh\{C_{g01}(V_{\rm gs} - C_{g01})\} \tag{14}$$

$$C_{\rm gs1} = C_{\rm gs14} + C_{\rm gs13} V_{\rm gs} + C_{\rm gs12} \tanh\{C_{\rm gs11}(V_{\rm gs} - C_{\rm gs11})\}. \tag{15}$$

Here C_{g0} is half the gate capacitance (average of $C_{\rm gs}$ and $C_{\rm gd}$) when the drain voltage is zero. $C_{\rm gd}$ and $C_{\rm ds}$ are also presented in same manner. In these equations, the drain bias dependence is presented by δ, which has the same linear-to-saturation transition characteristics as the dc characteristics. In these equations, the gate and the drain bias dependence can be defined independently.

The RF model is determined by the RF characteristics of various samples as measured by on-wafer 2-port S-parameter measurement in the range between 0.2 and 20 GHz with an HP8510 network analyzer. In the extraction, six parameters $(R_s, R_d, R_g, L_s, L_d, L_g)$ are fixed by the S-parameter measurements under the condition of forward gate current operation. Next, the other parameters are determined for minimal error of the S-parameters. The typical S-parameter error using the equivalent circuit shown in Fig. 1 is less than 5% for wide bias conditions, but in the linear region, the error is slightly larger.

The measured and modeled transconductances are compared in Fig. 4. Introducing the DX-center-induced current source, accuracy is significantly increases, especially for larger gate biases. The errors for all voltages is decreased from 14% to 5% by introduce the new current source.

Fig. 5 compares modeled and measured S-parameters. The errors are mostly less than 20% for the linear region and 10% for the saturated region. These values are good enough, because the typical discrepancy between measured and modeled using equivalent circuit shown in Fig. 1 is about 5%, which is derived from simplified

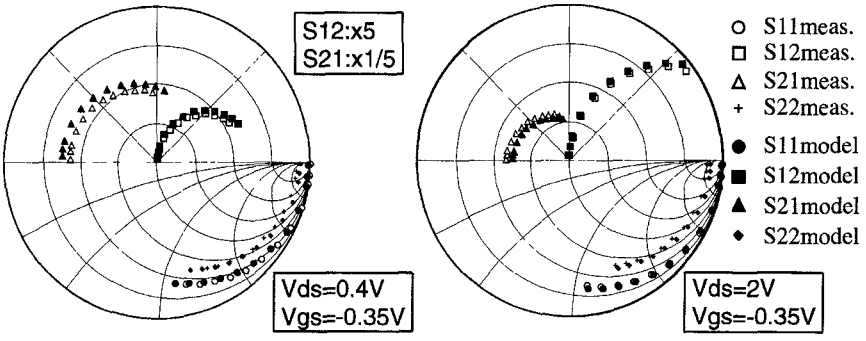

Fig. 5. Comparison of measured and modeled S-parameters. The left graph is typical characteristics in the linear region; the other is for the saturated region.

equivalent circuit, even for a certain bias condition in saturation region.

IV. Conclusion

A new nonlinear HEMT model is developed on the basis of the Curtice model for Harmonic Balance simulation. Terms for leakage current for subthreshold voltage, drain voltage dependence for knee voltage, drain conductance and threshold voltage, the transconductance enhancement by DX centers, and the bias dependence of capacitance are introduced. By adopting this model for a pseudomorphic double-recessed gate HEMT, average errors of 2.6% for dc current and 10% S-parameters are obtained.

References

[1] L. F. Lester, P. M. Smith, P. Ho, P. C. Chao, R. C. Tiberio, K. H. G. Duh, and E. D. Wolf, "0.15 μm gate length double recess pseudomorphic HEMT with F_{max} of 350 GHz," in *IEDM'88*, 1988, pp. 172–175.

[2] H. Daembkes, Ed., *Modulation-Doped Field-Effect Transistors: Applications and Circuits*. New York: IEEE Press, 1991.

[3] A. H. Ng, R. Khoie, and R. Venkat, "A two-dimensional self-consistent numerical model for high electron mobility transistor," *IEEE Trans. Electron Devices*, vol. 38, p. 852, 1991.

[4] W. R. Curtice and M. Ettenberg; "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, 1985.

[5] H. Rohdin and P. Roblin; "A MODFET DC model with improved pinchoff and saturation characteristics," *IEEE Trans. Electron Devices*, vol. ED-33, p. 664, 1986.

[6] T. Tanimoto, M. Kudo, T. Mishima, M. Mori, and M. Yamane, "Double recessed gate InGaAs pseudomorphic channel HEMT's for low current operation," ICICE Tech. Rep., vol. ED91-149, pp. 79–86, 1992 (in Japanese).

[7] H. Mizuta, K. Yamaguchi, M. Yamane, T. Tanoue, and S. Takahashi, "Two-dimensional numerical simulation of Fermi-level pinning phenomena due to DX centers in AlGaAs/GaAs HEMT's," *IEEE Trans. Electron Devices*, vol. 36, pp. 2307–2314, 1989.

Quasi-TEM Analysis of Coplanar Waveguides with an Inhomogeneous Semiconductor Substrate

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Abstract— **In this paper, we study the normalized wavelength and attenuation constant of coplanar waveguides with a finite metal thickness. The substrate is a lossy inhomogeneous insulator–semiconductor, and the conductor is assumed perfect. Electroquasi-static approximation is used to derive a Laplace's equation with a complex permittivity in each inhomogeneous layer, from which the eigenmodes are obtained. Proper boundary conditions between contiguous layers are applied to calculate the charge distribution on the center conductor. The effects of the insulator depth and semiconductor conductivity on the normalized wavelength and attenuation constant are analyzed.**

I. Introduction

The doping profile in the semiconductor substrate affects the propagation characteristics of microstrip lines and coplanar waveguides significantly. In [1] and [2], the propagation characteristics of coplanar waveguides fabricated on an insulator–semiconductor substrate have been studied. For Schottky-contact microstrip lines, the bias voltage applied to the metal line creates a localized depletion zone around the metallization [3]. Due to the conductive loss in the semiconductor, slow wave modes with attenuation are observed [3]–[8]. The slow wave factor and the attenuation constant of either microstrip lines or coplanar waveguides have been studied using parallel plate waveguide model [3], full-wave finite element method [6], finite-difference time-domain method [7], and method of lines [8].

As long as the cross-section dimension of the coplanar waveguide is a small fraction of one wavelength, the quasi-TEM analysis can be applied to model its propagation properties even up to the millimeter wave range. In [9], an electrostatic formulation is used to calculate the capacitance and inductance matrices on which the quasi-TEM analysis is based. Resistive loss due to imperfect conduct has been studied by using quasi-TEM approach [10] and conformal mapping technique [11]. In [12], both the semiconductor loss and conductor loss are considered. Overall, the inhomogeneities of substrate is only analyzed in [8].

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